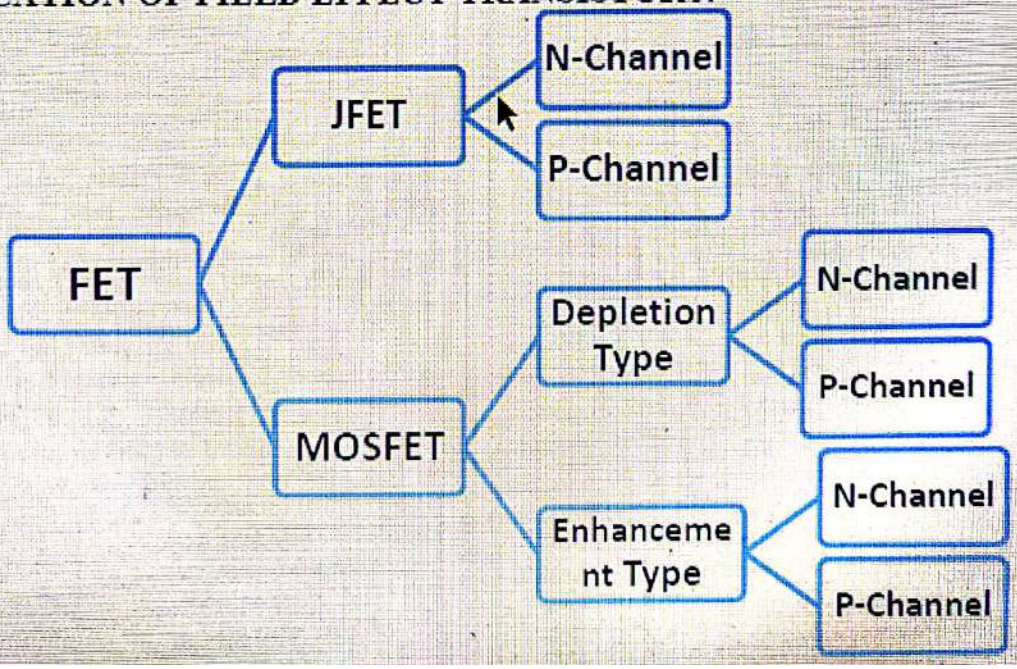
[FIELD EFFECT TRANSISTOR (FET)]

❖ INTRODUCTION: -

- In the previous chapters, we have discussed the circuit applications of an ordinary transistor. In this type of transistor, both holes and electrons play part in the conduction process. For this reason, it is sometimes called a Bipolar Transistor.
- The ordinary or bipolar transistor has two principal disadvantages. First, it has low input impedance because of forward biased emitter junction. Secondly, it has considerable noise level.
- Although low input impedance problem may be improved by careful design and use of more than one transistor, yet it is difficult to achieve input impedance more than a few mega ohms.
- The field effect transistor (FET) has, by virtue of its construction and biasing, large input impedance which may be more than 100 mega ohms.
- The FET is generally much less noisy than the ordinary or bipolar transistor. The rapidly expanding FET market has led many semiconductor marketing managers to believe that this device will soon become the most important electronic device, primarily because of its integrated-circuit applications.

❖ CLASSIFICATION OF FIELD EFFECT TRANSISTORS: -



❖ JUNCTION FIELD EFFECT TRANSISTOR (JFET) : -

➤ **A junction field effect transistor is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes.**

➤ **In a JFET, the current conduction is either by electrons or holes and is controlled by means of an electric field between the gate electrode and the conducting channel of the device.**

➤ **The JFET has high input impedance and low noise level.**

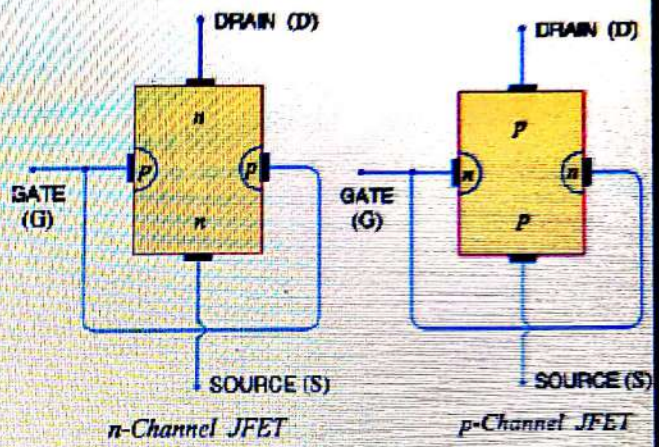
❖ CONSTRUCTIONAL DETAILS.

➤ A JFET consists of a p-type or n-type silicon bar containing two pn junctions at the sides as shown in Fig.

➤ The bar forms the conducting channel for the charge carriers. If the bar is of n-type, it is called n-channel JFET as shown in Fig (i) and if the bar is of p-type, it is called a p-channel JFET as shown in Fig (ii).

➤ The two pn junctions forming diodes are connected internally & a common terminal called gate is taken out.

➤ Other terminals are source and drain taken out from the bar as shown. Thus a JFET has essentially three terminals viz., Gate (G), Source (S) & Drain (D).



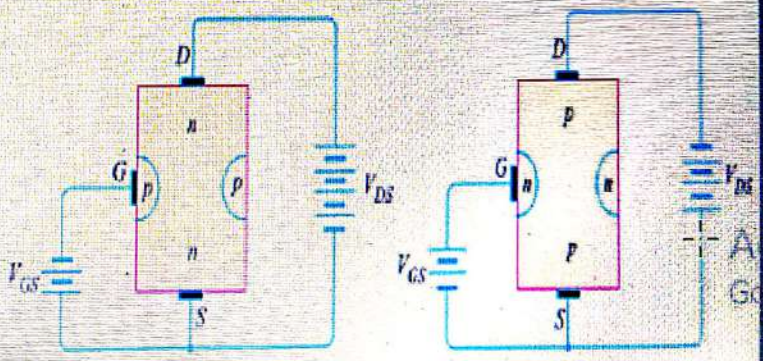
❖ JFET POLARITIES: -

➤ Fig (i) shows n-channel JFET polarities whereas Fig (ii) shows the p-channel JFET polarities.

➤ Note that in each case, voltage between gate and source is such that the gate is reversing biased.

➤ This is the normal way of JFET connection.

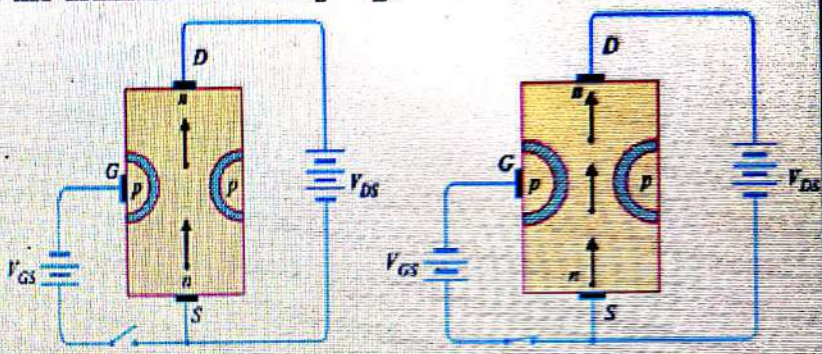
➤ The drain & source terminals are interchangeable i.e., either end can be used as source and the other end as drain.



- **The following points may be noted:**
  - **The input circuit (i.e. gate to source) of a JFET is reverse biased. This means that the device has high input impedance.**
  - **The drain is so biased w.r.t. source that drain current I_D flows from the source to drain.**
  - **In all JFETs, source current I_S is equal to the drain current i.e. $I_S = I_D$.**

❖ WORKING PRINCIPLE OF JFET:-

Principle: - Fig. shows the circuit of n-channel JFET with normal polarities. Note that the gate is reverse biased.

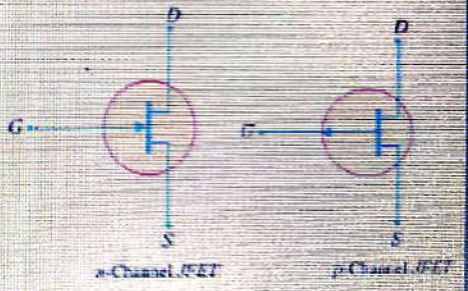


- The two pn junctions at the sides form two depletion layers. The current conduction by charge carriers (i.e. free electrons in this case) is through the channel between the two depletion layers and out of the drain.
- The width and hence resistance of this channel can be controlled by changing the input voltage V_{GS}.
- The greater the reverse voltage V_{GS}, the wider will be the depletion layers and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen should V_{GS} decrease.
- Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}.
- In other words, the magnitude of drain current (I_D) can be changed by altering V_{GS}.

Working: - The working of JFET is as under :

- (i) When voltage V_{DS} is applied between drain & source terminals and voltage on the gate is zero [See the above Fig (i)], the two pn junctions at the sides of the bar establish depletion layers.
- The electrons will flow from source to drain through a channel between the depletion layers.

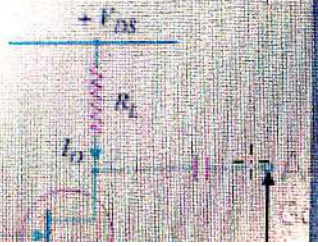
- **The size of these layers determines width of the channel & hence current conduction through the bar.**
- **(ii) When a reverse voltage V_{GS} is applied between the gate and source [See Fig (ii)], the width of the depletion layers is increased.**
- **This reduces the width of conducting channel, thereby increasing the resistance of n-type bar. Consequently, the current from source to drain is decreased.**
- **On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain current.**
- **It is clear from the above discussion that current from source to drain can be controlled by the application of potential (i.e. electric field) on the gate.**
- **For this reason, the device is called field effect transistor. It may be noted that a p-channel JFET operates in the same manner as an n-channel JFET except that channel current carriers will be the holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.**



[Schematic Symbol of JFET]

❖ JFET AS AN AMPLIFIER :-

- Fig shows JFET amplifier circuit. The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit. For the proper operation of JFET, the gate must be negative w.r.t. source i.e., input circuit should always be reverse biased.
- This is achieved either by inserting a battery V_{GG} in the gate circuit or by a circuit known as biasing circuit.
- In the present case, we are providing biasing by the battery V_{GG}. A small change in the reverse bias on the gate produces a large change in drain current.
- This fact makes JFET capable of raising the strength of a weak signal. During the positive half of signal, the reverse bias on the gate decreases. This increases the channel width and hence the drain current.
- During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases.



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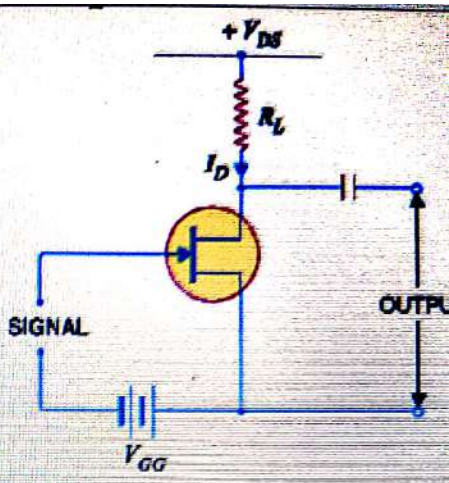
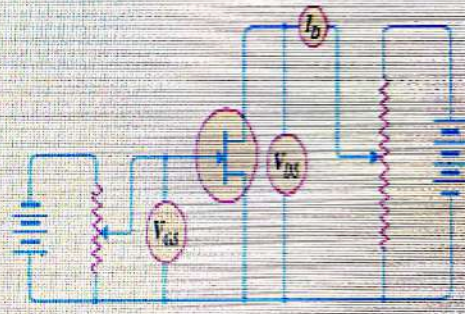
- During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases.
- The result is that a small change in voltage at the gate produces a large change in drain current.
- These large variations in drain current produce large output across the load R_L. In this way, JFET acts as an amplifier



❖ OUTPUT CHARACTERISTICS OF JFET

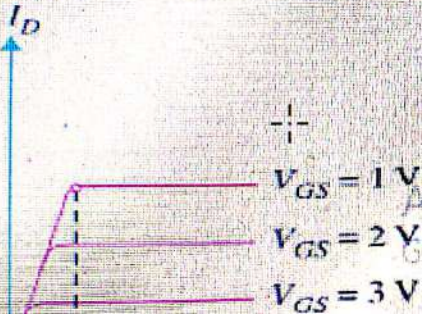
- The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a JFET at constant gate source voltage (V_{GS}) is known as output characteristics of JFET.
- Fig shows circuit for determining output characteristics of JFET.
- Keeping V_{GS} fixed at some value, say 1V, the drain source voltage is changed in steps.
- Corresponding to each value of V_{DS}, the drain current I_D is noted.
- A plot of these values gives output characteristic of JFET at V_{GS}= 1V.



- Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. shows a family of output characteristics.

The following points may be noted from the characteristics:

- (i) At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant.
- The drain-source voltage above which drain current becomes constant is known as pinch off voltage. Thus in Fig. OA is the pinch off voltage V_P.
- (ii) After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other.
- The drain current passes through the small passage between these layers.
- Thus increase in drain current is very small with V_{DS} above pinch off voltage.



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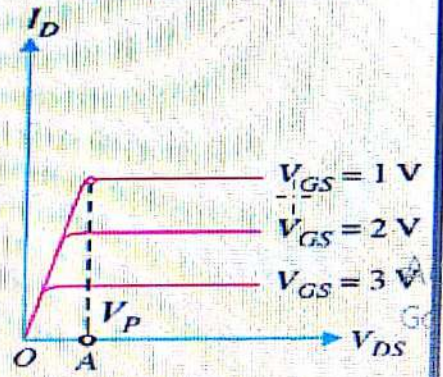
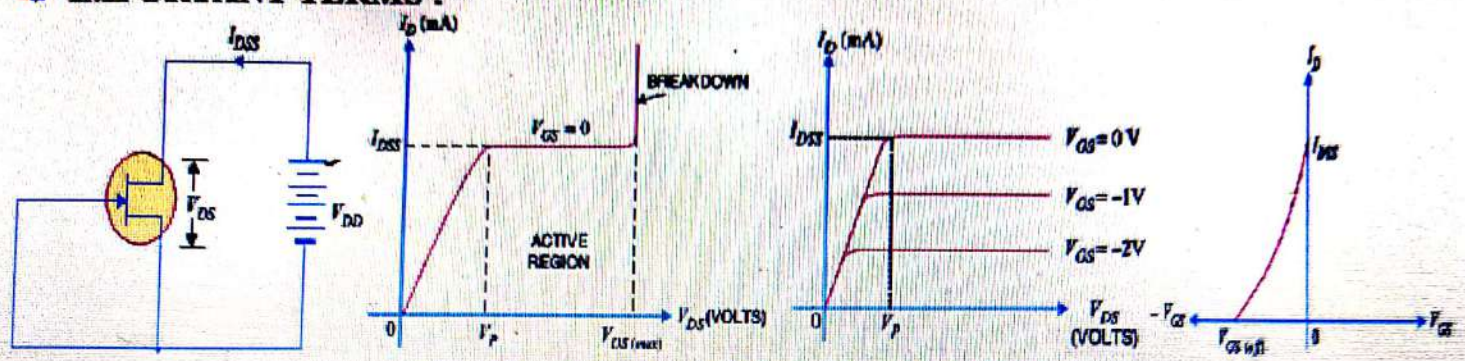
- The drain current passes through the small passage between these layers.
- Thus increase in drain current is very small with V_{DS} above pinch off voltage.
- Consequently, drain current remains constant. The characteristics resemble that of a pentode valve.



IMPORTANT TERMS : -



1. Shorted-Gate Drain Current (I_{DSS}): -

➤ It is the drain current with source short-circuited to gate (i.e. $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage. It is sometimes called zero-bias current.

2. Pinch Off Voltage (V_P) : -

➤ It is the minimum drain-source voltage at which the drain current essentially becomes constant.

3. Gate-Source Cut Off Voltage V_{GS} (off): -

➤ It is the gate-source voltage where the channel is completely cut off & the drain current becomes zero.

❖ PARAMETERS OF JFET: -

➤ Like vacuum tubes, a JFET has certain parameters which determine its performance in a circuit. The main parameters of JFET are: - (i) A.C. drain resistance (ii) Transconductance (iii) Amplification factor.

♣ (i) <u>A.C. Drain Resistance</u> (r_d). Corresponding to the a.c. plate resistance, we have a.c. drain resistance in a JFET. It may be defined as follows :

➤ It is the ratio of change in drain-source voltage (ΔV_{DS})to the change in drain current(ΔI_D) at constant gate-source voltage i.e.

$$\text{A.C. Drain Resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}$$

- For instance, if a change in drain voltage of 2 V produces a change in drain current of 0.02 mA, then, a.c. drain resistance, $r_d = \frac{2V}{0.02\ mA} = 100\ k\Omega$
- Referring to the output characteristics of a JFET in Fig., it is clear that above the pinch off voltage, the change in I_D is small for a change in V_{DS} because the curve is almost flat.
- Therefore, drain resistance of a JFET has a large value, ranging from 10 kΩ to 1 MΩ.
- (ii) **Transconductance** (g_{fs}) : -The control that the gate voltage has over the drain current is measured by transconductance g_{fs} & is similar to transconductance g_m of the tube. It may be defined as follows: -
- It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage(ΔV_{GS}) at constant drain-source voltage i.e.

$$\text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

- The transconductance of a JFET is usually expressed either in mA/volt or micro mho. As an example, if a change in gate voltage of 0.1 V causes a change in drain current of 0.3 mA, then, Transconductance,
  → $g_{fs} = \frac{0.3\ mA}{0.1\ V} = 3mA/V = 3\times10^{-3}$ A/V or mho or S(Siemens)$=3\times10^{-3}\times10^{6}$ μ mho = 3000 μ mho (or μS)
- (iii) **Amplification Factor** (μ). It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage(ΔV_{GS}) at constant drain current i.e.

$$\text{Amplification Factor, } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D$$

- Amplification factor of a JFET indicates how much more control the gate voltage has over drain current than has the drain voltage.

❖ RELATION AMONG JFET PARAMETERS: -

➢ **The relationship among JFET parameters can be established as under :**

We know $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$

➢ **Multiplying the numerator and denominator on R.H.S. by ΔI_D, we get,**

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$ ➔ $\mu = r_d \times g_{fs}$

➔ **Amplification Factor = A.C. Drain Resistance × Transconductance**

❖ JFET BIASING: -

➢ For the proper operation of n-channel JFET, gate must be negative w.r.t. source. This can be achieved either by inserting a battery in the gate circuit or by a circuit known as biasing circuit.

➢ The latter method is preferred because batteries are costly and require frequent replacement.

1. Bias Battery: - In this method, JFET is biased by a bias battery V_{GG}. This battery ensures that gate is always negative w.r.t. source during all parts of the signal.

2. Biasing circuit: -The biasing circuit uses supply voltage V_{DD} to provide the necessary bias. Two most commonly used methods are (i) Self-Bias (ii) Potential Divider Method.

❖ SELF-BIAS FOR JFET : -

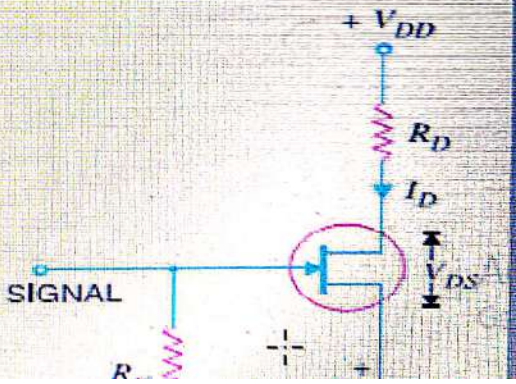
➢ Fig shows the self-bias method for n-channel JFET. The resistor RS is the bias resistor.

➢ The d.c. component of drain current flowing through R_S produces the desired bias voltage.

Voltage across R_S, $V_S = I_D R_S$

➢ Since gate current is negligibly small, the gate terminal is at d.c. ground i.e., $V_G = 0$.

$\therefore \quad V_{GS} = V_G - V_S = 0 - I_D R_S \quad$ or $\quad V_{GS} = -I_D R_S$



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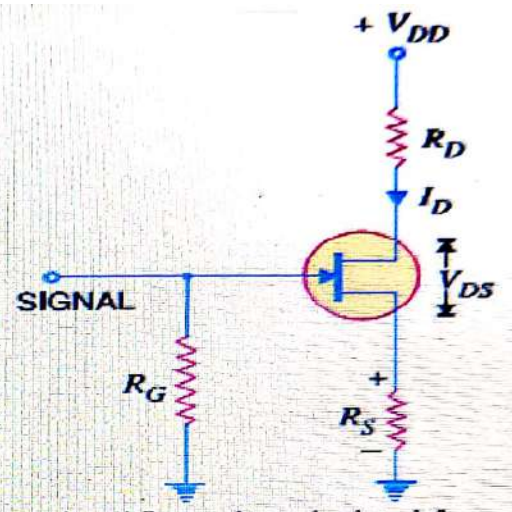

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- Thus bias voltage V_{GS} keeps gate negative w.r.t. source.

Operating point: -

- The operating point (i.e., zero signals I_D & V_{DS}) can be easily determined. Since the parameters of the JFET are usually known, zero signal I_D can be calculated from the following relation :

$$I_D = I_{DSS}\left(1 - \frac{\Delta V_{GS}}{\Delta V_{GS(off)}}\right)^2$$

Also $\quad V_{DS} = V_{DD} - I_D (R_D + R_S)$

- Thus d.c. conditions of JFET amplifier are fully specified i.e. operating point for the circuit is (V_{DS}, I_D).

Also, $\quad R_S = \dfrac{|V_{GS}|}{|I_D|}$

- Note that gate resistor R_G does not affect bias because voltage across it is zero.

Midpoint Bias: -

It is often desirable to bias a JFET near the midpoint of its transfer characteristic curve where $I_D = I_{DSS}/2$. When signal is applied, the midpoint bias allows a maximum amount of drain current swing between I_{DSS} and 0.

- It can be proved that when $V_{GS} = V_{GS\,(off)} / 3.4$, midpoint bias conditions are obtained for I_D.

$$I_D = I_{DSS}\left(1 - \frac{\Delta V_{GS}}{\Delta V_{GS(off)}}\right)^2 = I_{DSS}\left(1 - \frac{\Delta V_{GS(off)}/3.4}{\Delta V_{GS(off)}}\right)^2 = 0.5\, I_{DSS}$$

- To set drain voltage at midpoint ($V_D = V_{DD}/2$), select a value of R_D to

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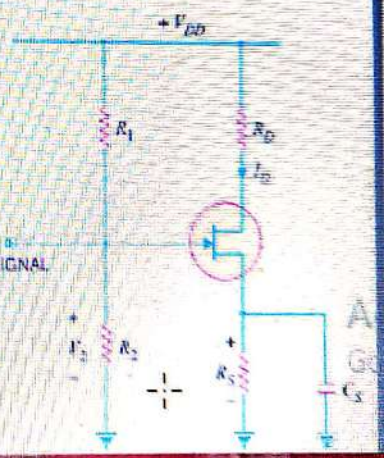
- To set drain voltage at midpoint ($V_D = V_{DD}/2$), select a value of R_D to produce the desired voltage drop.



❖ JFET with Voltage-Divider Bias :-

- Fig shows potential divider method of biasing a JFET. This circuit is identical to that used for a transistor.
- The resistors R_1 and R_2 form a voltage divider across drain supply V_{DD}. The voltage V_2 (= V_G) across R_2 provides the necessary bias.

$$V_2 = V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

Now $V_2 = V_{GS} + I_D R_S$ **Or** $V_{GS} = V_2 - I_D R_S$

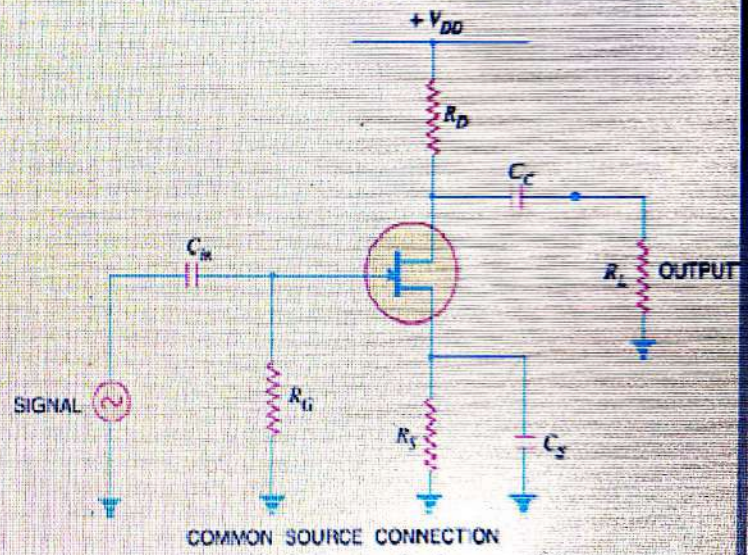
- **The circuit is so designed that $I_D R_S$ is larger than V_2 so that V_{GS} is negative. This provides correct bias voltage. We can find the operating point as under:**

$$I_D = \frac{V_2 - V_{GS}}{R_S} \quad \text{and} \quad V_{DS} = V_{DD} - I_D (R_D + R_S)$$

- **Although the circuit of voltage-divider bias is a bit complex, yet the advantage of this method of biasing is that it provides good stability of the operating point.**
- **The input impedance Z_i of this circuit is given by ;** $Z_i = R_1 \| R2$

❖ JFET Connections: -

- **There are three leads in a JFET viz., source, gate and drain terminals. However, when JFET is to be connected in a circuit, we require four terminals; two for the input and two for the output.**
- This difficulty is overcome by making one terminal of the JFET common to both input and output terminals. Accordingly, a JFET can be connected in a circuit in the following three ways:
  - ♣ Common Source connection
  - ♣ Common Gate connection
  - ♣ Common Drain connection
- The common source connection is the most widely used arrangement. It is because this connection provides high input impedance, good voltage gain and moderate output impedance.



COMMON SOURCE CONNECTION

- However, the circuit produces a phase reversal i.e., output signal is 180° out of phase with the input signal. Fig. shows a common source n-channel JFET amplifier.
- Note that source terminal is common to both input and output.

JFET Applications : -

The high input impedance and low output impedance and low noise level make JFET far superior to the bipolar transistor. Some of the circuit applications of JFET are :

- As a Buffer amplifier
- As Phase-shift oscillators
- As RF amplifier